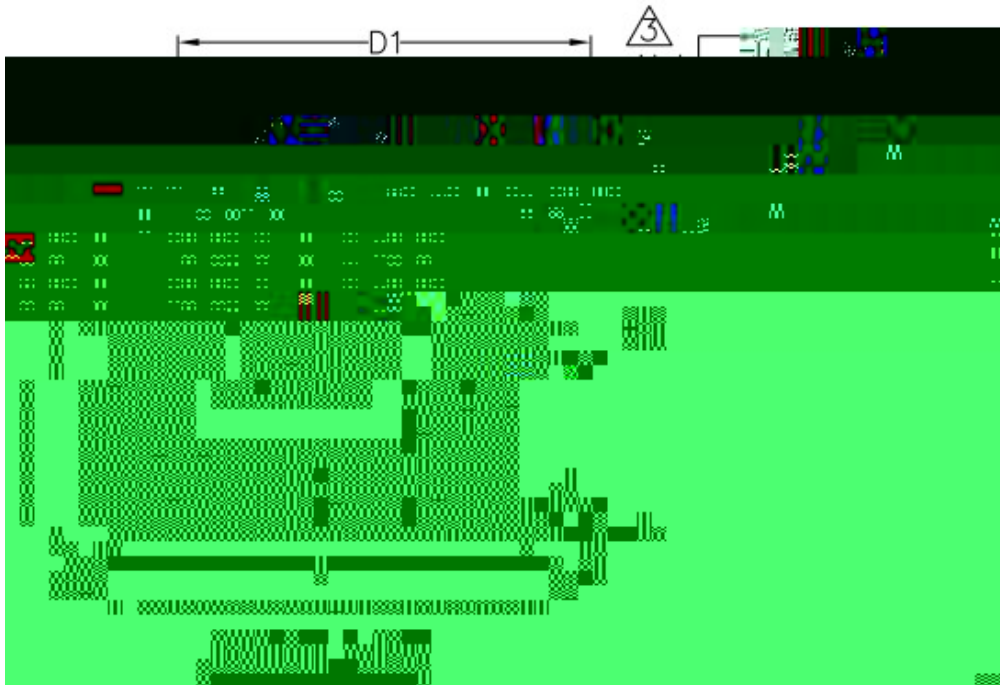
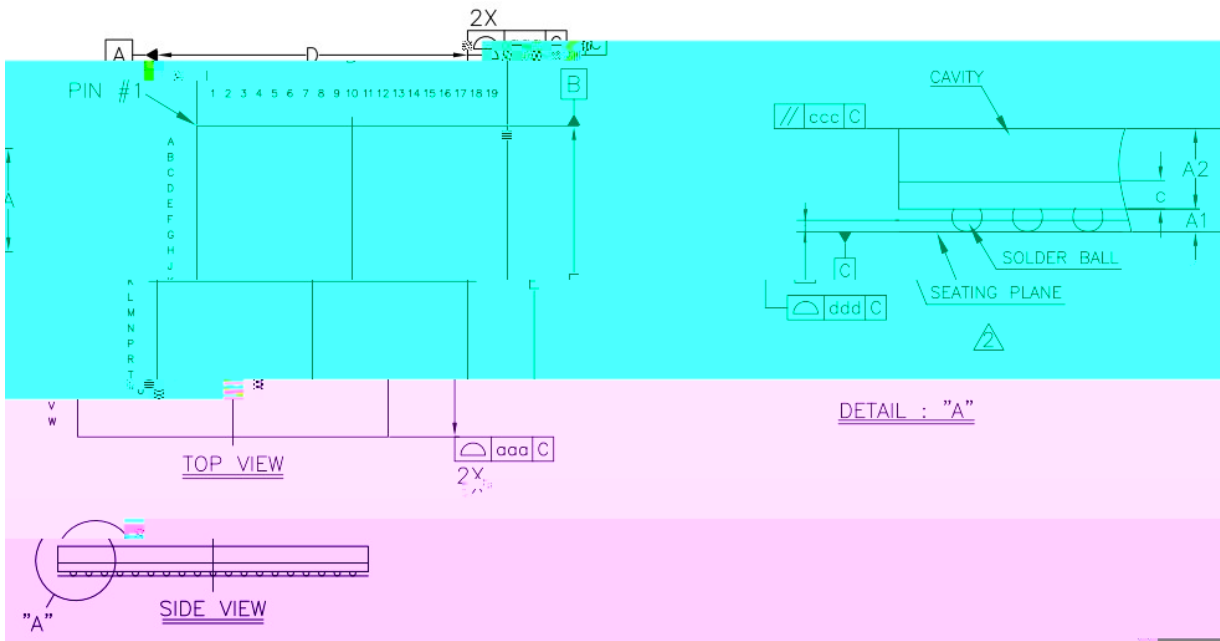
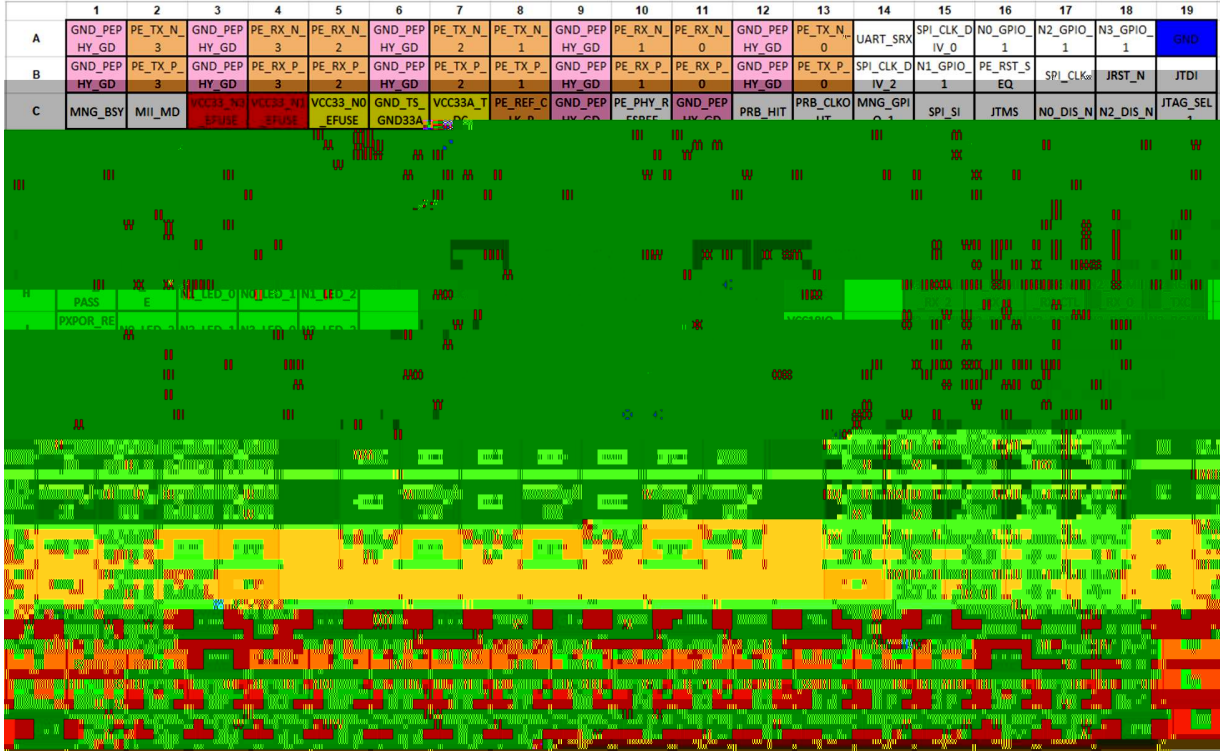


Table of Contents









Ω









W €)

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W s r dds







31

	-65		140	° C
Tj(FN)	-55		125	° C
VCK VCI1A	-01	11	115	V
VCI1A_FE; VCI1A_AIO VCI1A_CEN; VCI1A_HL	-01	11	115	V
VCI1Q; VCI3A VCI3	-04	33	37	V
VCI1O; VCI25V	-04	33	37	V

32

	-40		85	° C
VCK VCI1A	105	11	115	V
VCI1A_FE; VCI1A_AIO VCI1A_CEN; VCI1A_HL	105	11	115	V
VCI1Q; VCI3A VCI3	315	33	345	V
VCI1O; VCI25V	315	33	345	V

33

IOreference vdtage	Vref		30	33	36	V
Input low vdtage	Vl				08	V
Input high vdtage	Vh		20			V
Input low current	Iil	Vin=0V	-20		0	μA
Input high current	Iih	Vin=Vref- Vref, max	0		200	μA
Output low vdtage	Vl	Id=-4mA Vref=rin	0		400	nW
Output high vdtage	Vh	ICh=- 4mA Vref=rin	24		Vref	V

34

3.1.1 NCSI AC Specification

T_{clk}	NSI_REF_CLK Frequency		50		NE
R_{clk}	NSI_REF_CLK duty cycle	35		65	%
R_{acc}	NSI_REF_CLK accuracy			100	ppm
T_{to}	Clock to out (10 pF \times load \leq 50 pF) NSI_TQ1:Q , NSI_SRIV Data valid from NSI_REF_CLK rising edge	2.5		12.5	ns
T_{su}	NSI_TQ1:Q , NSI_TXEN Data Setup to NSI_CLKIN rising edge	3			ns
T_{hdd}	NSI_TQ1:Q , NSI_TXEN Data hold from NSI_REF_CLK rising edge	1			ns
T_r	NSI_TQ1:Q , NSI_SRIV Output Time rise	0.5		6	ns
T_f	NSI_TQ1:Q , NSI_SRIV Output Time fall	0.5		6	ns
T_{dr}/T_{df}	NSI_REF_CLK Rise/Fall Time	0.5		3.5	ns

34

Frequency	-	-	25	-	NE
Frequency Stability	T_a=0 70	-30		+30	ppm
Frequency Tolerance	T_a=25	-50		+50	ppm
Duty Cycle		40		60	%
Broadband Peak to peak Jitter				200	ps
V_{peak to peak}		3.135	3.3	3.465	V



Rise time 10%90%				10	ns
Fall time 10%90%				10	ns
Operation temperature Range		0		70	

35

CHY IP **1 IV** **33V 5ms** **33V rise time** **1ns**
33V **1 IV**

R1	33V rise time	1	-	
R3	IV 33V ready to 1 IV ready time	-5	-	

virbond	V5Q0V
microchip	SS125AF080B
	CD5Q0

1	VN8002		0 - 70 , 4m2	2
2	VN8002S		0 - 70 , 4m2 , SM/SN/SM	2
3	VN8004		0 - 70 , 4m4	4
4	VN8004S		0 - 70 , 4m4 , SM/SN/SM	4
5	VN8002L2		-40 - 85 , 4m2	2
6	VN8002LS		-40 - 85 , 4m2 , SM/SN/SM	2
7	VN8004L4		-40 - 85 , 4m4	4
8	VN8004LS		-40 - 85 , 4m4 , SM/SN/SM	4

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